Listing of Claims

No amendments are being presented to the claims at this time. This listing of claims is provided merely for convenience, and will replace all prior versions and listings of claims in the application.

1. (Original) A method, comprising:

controlling an electrical load with a first code executed by a processor;

releasing processor control so that the electrical load operates in an open control mode while the first code is displaced with a second code; and

reinstating processor control of the electrical load using the second code.

2. (Original) The method of claim 1, wherein the first code of the controlling step is supplied from a boot read only memory (ROM).

3. (Original) The method of claim 1, wherein the controlling step comprises loading the first code into a first memory location accessed by the processor.

4. (Original) The method of claim 3, wherein the controlling step further comprises loading the second code into a second memory location accessible by the processor.

5. (Original) The method of claim 4, wherein the releasing step comprises moving the second code from the second memory location into the first memory location, thereby displacing the first code from the first memory location.

6. (Original) The method of claim 1, wherein the electrical load is a motor.

7. (Original) The method of claim 6, wherein the motor supports a data storage medium, and wherein the controlling step comprises using the motor to rotate the data storage medium at an operational velocity and retrieving the second code from the rotating data storage medium.

8. (Previously presented) A method, comprising:

using a processor to execute startup code loaded into a memory location to initiate operational control of an electrical load;

continuing to operate the electrical load while processor operational control of the electrical load is temporarily suspended to load application code to the memory location; and

resuming operational control of the electrical load using the application code.

9. (Original) The method of claim 8, wherein the startup code of the using step is supplied from a boot read only memory (ROM).

10. (Original) The method of claim 8, wherein the memory location of the using step is characterized as a first memory location, and wherein the using step further comprises loading the application code into a second memory location accessible by the processor.

11. (Original) The method of claim 10, wherein the continuing step comprises moving the application code from the second memory location into the first memory location, thereby displacing the startup code from the first memory location.

12. (Original) The method of claim 8, wherein the electrical load comprises a motor supporting a data storage medium, and wherein the using step comprises energizing the motor to rotate the data storage medium at an operational velocity and retrieving the application code from the rotating data storage medium.

13. (Original) The method of claim 12, wherein the using step further comprises using the startup code to energize an actuator motor to bring a data transducing head into alignment with a track defined on the data storage medium, and utilizing the head to transduce the application data from said track.

14. (Previously presented) An apparatus, comprising:

an electrical load;

a memory location; and

a programmable processor coupled to the memory location and adapted to control the electrical load, wherein during an initialization process the processor executes startup code loaded into the memory location to initiate operational control of the load, temporarily releases operational control of the electrical load so that the electrical load continues to operate in an open control mode

while application code is loaded to the memory location, and resumes operational control of the electrical load using the application code.

15. (Original) The apparatus of claim 14, further comprising a boot read only memory (ROM) which stores the startup code, wherein the startup code is loaded from the boot ROM to the memory location for execution by the processor.

16. (Original) The apparatus of claim 14, wherein the memory location of the using step is characterized as a first memory location, and wherein the apparatus further comprises a second memory location accessible by the processor and into which the processor loads the application code.

17. (Original) The apparatus of claim 14, wherein the electrical load comprises a motor supporting a data storage medium, and wherein the execution of the startup code by the processor results in the energizing of the motor to rotate the data storage medium at an operational velocity.

18. (Original) The apparatus of claim 17, further comprising an actuator motor coupled to a data transducing head, and wherein the execution of the startup code by the processor further results in the energizing of the actuator motor to bring the head into alignment with a track defined on the data storage medium, the head transducing the application data from said track.

19. (Previously presented) The method of claim 1 wherein the processor operationally controls the electrical load.

20. (Previously presented) The method of claim 1, wherein at least one control signal is applied to the electrical load during the open control mode of the releasing step.